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| 09/923,997 | 08/07/2001 | Hiroyuki Takahashi | SIM-01501 | 1911 |

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| EXAMINER |
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| COX, CASSANDRA F |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2816 | |

DATE MAILED: 02/15/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/923,997 | TAKAHASHI, HIROYUKI | |
| | Examiner | Art Unit | |
| | Cassandra Cox | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sh et with th correspondenc address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *07 August 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9-12 and 15-17* is/are rejected.

7)☒ Claim(s) *7,8,13 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

### *Specification*

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5, 9-11, and 15-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Hattori (U.S. Patent No. 5,459,424).

In reference to claim 1, Hattori discloses in Figure 1 a delay circuit for delaying a logic signal (at input I) having two logic levels consisting of a low level and a high level, comprising: an inverter chain (21, 22) containing not less than one inverter; and a metal-oxide-semiconductor capacitor (27, 28), known as a MOS capacitor (see column 1, lines 35-37) connected to an output section of the inverter (21) and, when a logic signal having a targeted logic level is input, changes from an off-state to an on-state during a transition period of a signal that appears in the output section of the inverter. The same applies to claims 2 and 16.

In reference to claim 3, because the claimed structure is fully met by Hattori, the recited function or "result" limitation "wherein a ratio of a gate voltage range of an on-state MOS capacitor to a gate voltage range of an off-state MOS capacitor is proportional to an increment or a decrement of the source voltage during a transition period of a signal that appears in the output section of the inverter" will necessarily be inherent in Hattori, as held by the court in In re Best, 195 USPQ 430. The same applies to claim 9.

In reference to claim 4, because the claimed structure is fully met by Hattori, the recited function or "result" limitation "wherein a value of the MOS capacitor changes in a direction to increase its capacitance during a transition period of a signal that appears in the output section of the inverter" will necessarily be inherent in Hattori, as held by the court in In re Best, 195 USPQ 430. The same applies to claims 10 and 17.

In reference to claim 5, Hattori discloses in Figure 1 that the MOS capacitor is disposed on a transmission path of a logic signal, and is represented by an n-MOS transistor (28) whose gate is connected to a node that changes a logic level of the logic signal from a low level to a high level, and whose source and whose drain are fixed at a ground potential (GND). The same applies to claim 11.

In reference to claim 15, Hattori discloses in Figure 1 a delay circuit for delaying a logic signal (at input I) having two logic levels consisting of a low level and a high level, comprises: an inverter chain (21, 22) containing not less than one inverter; and a p-channel metal-oxide-semiconductor transistor (23) and an n- channel metal-oxide-semiconductor transistor (24), known as MOS transistors, to comprise the inverter (see

column 1, lines 20-32), wherein a gate threshold voltage of each gate is shifted in mutually opposing directions.

4. Claims 1-4, 9-10, and 16-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Usuki et al. (U.S. Patent No. 5,006,738).

In reference to claim 1, Usuki discloses in Figure 5 a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprising: an inverter chain (51, 52, 53, 54) containing not less than one inverter; and a metal-oxide-semiconductor capacitor (55, 56, 57, 58), known as a MOS capacitor (see column 1, lines 20-26) connected to an output section of the inverter (51-54) and, when a logic signal having a targeted logic level is input, changes from an off-state to an on-state during a transition period of a signal that appears in the output section of the inverter. The same applies to claims 2 and 16.

In reference to claim 3, because the claimed structure is fully met by Usuki, the recited function or "result" limitation "wherein a ratio of a gate voltage range of an on-state MOS capacitor to a gate voltage range of an off-state MOS capacitor is proportional to an increment or a decrement of the source voltage during a transition period of a signal that appears in the output section of the inverter" will necessarily be inherent in Usuki, as held by the court in In re Best, 195 USPQ 430. The same applies to claim 9.

In reference to claim 4, because the claimed structure is fully met by Usuki, the recited function or "result" limitation "wherein a value of the MOS capacitor changes in a direction to increase its capacitance during a transition period of a signal that appears in

the output section of the inverter" will necessarily be inherent in Usuki, as held by the court in In re Best, 195 USPQ 430. The same applies to claims 10 and 17.

> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

5. Claims 1-6, 9-12, and 16-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Porter et al. (U.S. Patent No. 6,040,713).

In reference to claim 1, Porter discloses in Figure 11 a delay circuit for delaying a logic signal (at input FB12) having two logic levels consisting of a low level and a high level, comprising: an inverter chain (92, 94, 96, 98, 100) containing not less than one inverter; and a metal-oxide-semiconductor capacitor (102, 104, 106, 108), known as a MOS capacitor (see column 6, lines 34-36) connected to an output section of the inverter (92, 94, 96, 98, 100) and, when a logic signal having a targeted logic level is input, changes from an off-state to an on-state during a transition period of a signal that appears in the output section of the inverter. The same applies to claims 2 and 16.

In reference to claim 3, because the claimed structure is fully met by Porter, the recited function or "result" limitation "wherein a ratio of a gate voltage range of an on-state MOS capacitor to a gate voltage range of an off-state MOS capacitor is proportional to an increment or a decrement of the source voltage during a transition period of a signal that appears in the output section of the inverter" will necessarily be

inherent in Porter, as held by the court in In re Best, 195 USPQ 430. The same applies to claim 9.

In reference to claim 4, because the claimed structure is fully met by Porter, the recited function or "result" limitation "wherein a value of the MOS capacitor changes in a direction to increase its capacitance during a transition period of a signal that appears in the output section of the inverter" will necessarily be inherent in Porter, as held by the court in In re Best, 195 USPQ 430. The same applies to claims 10 and 17.

In reference to claim 5, Porter discloses in Figure 11 that the MOS capacitor is disposed on a transmission path of a logic signal, and is represented by an n-MOS transistor (92, 94, 96, 98, 100) whose gate is connected to a node that changes a logic level of the logic signal from a low level to a high level, and whose source and whose drain are fixed at a ground potential. The same applies to claim 11.

In reference to claim 6, Porter discloses in column 6, lines 39-45 that the MOS capacitor (92, 94, 96, 98, 100) could also be represented by a p-MOS transistor whose gate is connected to a node that changes a logic level of the logic signal from a high level to a low level, and whose source and drain are fixed at a ground potential. The same applies to claim 12.

***Allowable Subject Matter***

6. Claims 7-8 and 13-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: Claims 7 and 13 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 3 wherein the MOS capacitor is represented by an n-MOS transistor whose source and drain are connected to a node that changes a logic level of the logic signal from a high level to a low level, and whose gate is fixed at a source voltage in combination with the rest of the limitations of the base claims and any intervening claims.

Claims 8 and 14 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 3 wherein the MOS capacitor is represented by a p-MOS transistor whose source and drain are connected to a node that changes a logic level of the logic signal from a high level to a low level, and whose gate is fixed at a ground potential in combination with the rest of the limitations of the base claims and any intervening claims.

***Conclusion***

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ibaraki (U.S. Patent No. 5,124,574), Tanaka et al. (U.S. Patent No. 4,970,694), Watanabe et al. (U.S. Patent No. 5,055,713), and Stave (U.S. Patent No. 6,154,078) all disclose delay circuits having an inverter chain and a capacitor connected to an output section of the inverter.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 703-306-

5735. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (703)-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

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February 8, 2002

Kenneth B. Wells
Primary Examiner